Development of Multi-pixel THz Receivers

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Outline

- **Multi-pixel Receivers: why do we need them?**
- **Technical Approach**
- **Array Receivers**
  - Mixers
  - LO subsystem
  - Back-ends
  - Receiver system
- **Summary**

Filamentary Structure and Star Formation

Determining Characteristics of Filaments & Required Probes

KINEMATICS: ^{13}CO

DENSITIES: multiple transitions of ^{13}CO, $C^{18}O$, HCN & others

TEMPERATURE: ^{12}CO, NH_3

MAGNETIC FIELD: submm dust polarization (HAWC+)

MASS ACCRETION: C^+

The extinction in regions around filaments is low so that carbon is likely in the form of C^+

Velocity shifts of few tenths of km/s expected

LARGE-SCALE HIGH VELOCITY RESOLUTION IMAGES OF MANY SQ. ARCMIN. REGIONS ARE ESSENTIAL

Central portion of Taurus in ^{13}CO with ang. res. $\Delta\Theta = 50''$

Herschel observations have established the ubiquity of filaments

Stars form in dense condensations within filaments

But what controls formation of filaments and their evolution?

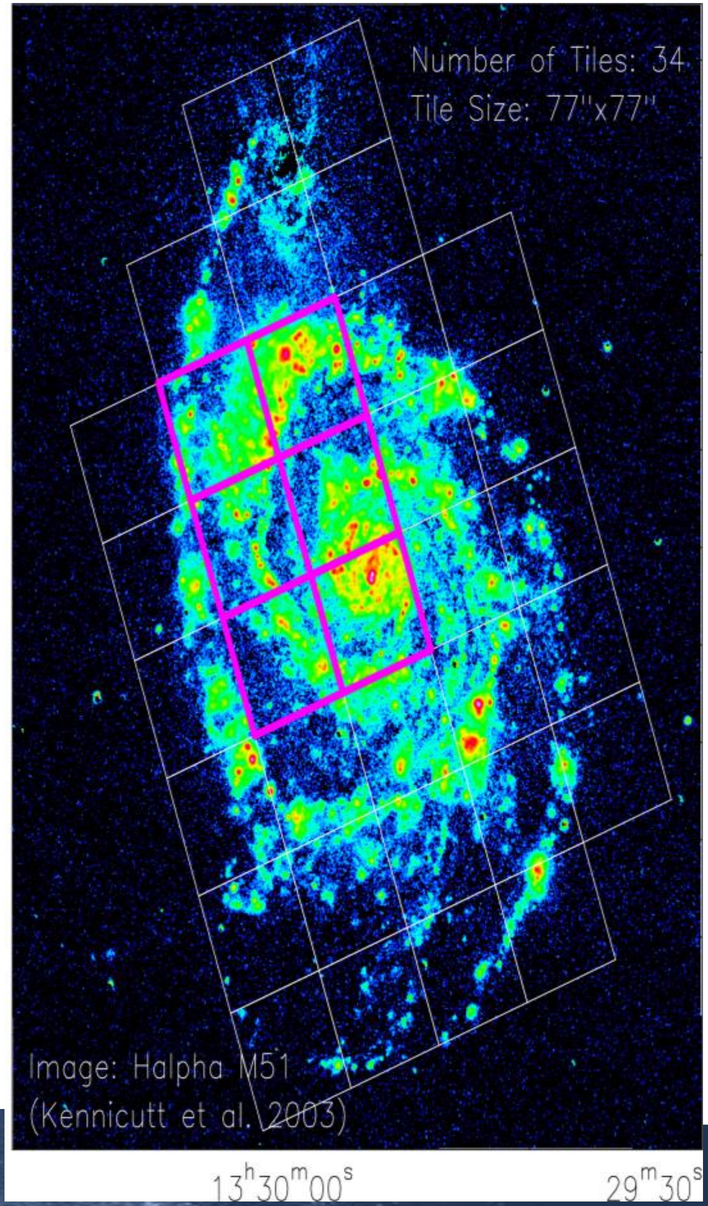
And most importantly, what determines when they get to point of fragmentation into CORES which then form new stars?

Even Nearby Galaxies Require Higher Angular Resolution than 1' Available from Balloons

Spiral Galaxies

Key questions

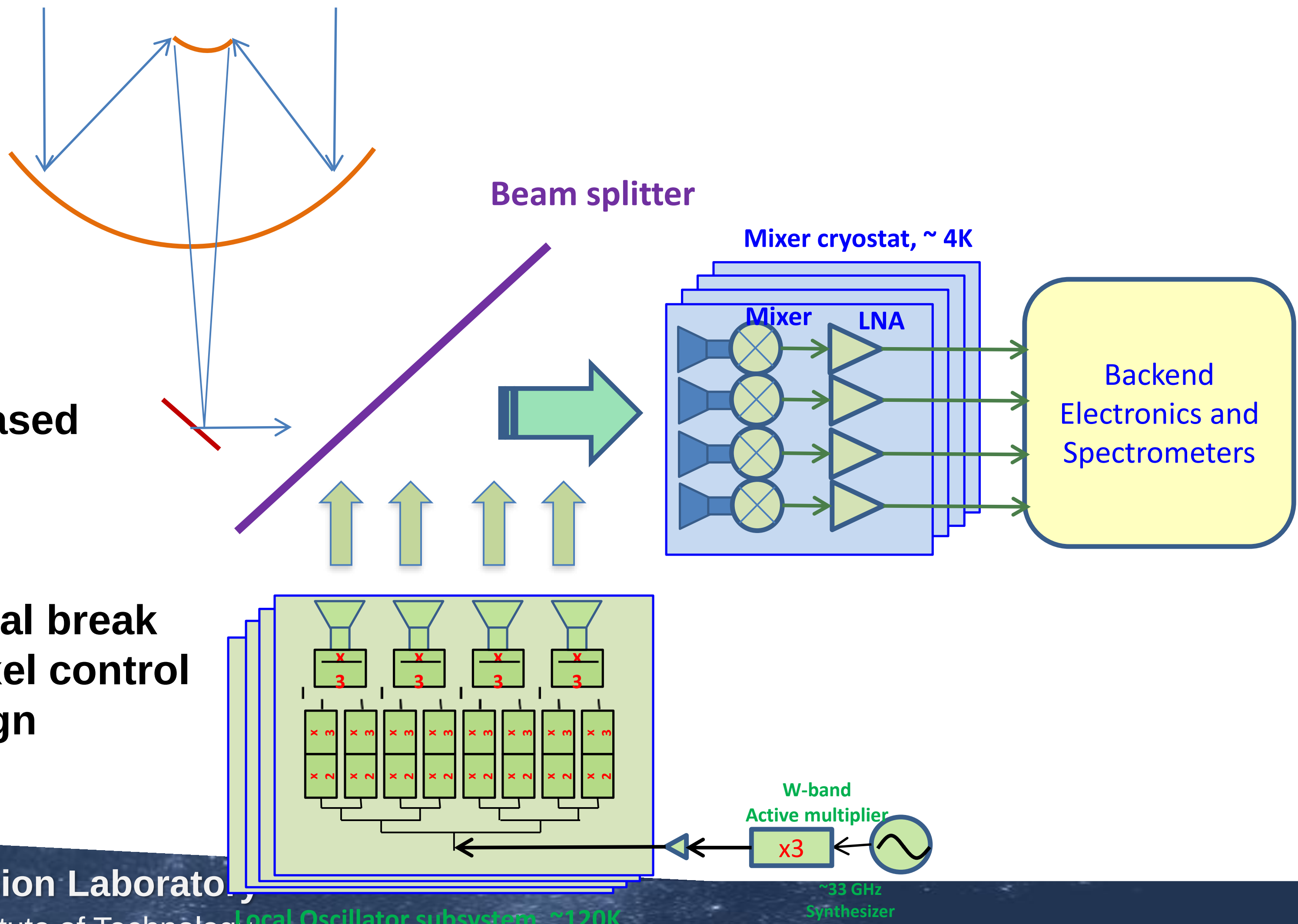
- How do spiral arms compress gas and initiate star formation?
- What is the nature of the interstellar medium in the interarm regions – the starting point for next generation of stars?
- How much, and where is the ``CO-Dark Molecular Gas''?
  SOFIA CYCLE 4 ``Impact'' Project
  (J. Pineda, US PI; joint with Germany)
  Map M15 in [CII] 158 μm line with upGREAT and FIFI-LS
  Ang. Res. = 16" = 540 pc (good but not enough to really resolve interstellar clouds)
  60 hr upGREAT+ 15 hr FIFI-LS
  2 yr; 15 flights
- **ARRAY WITH >> 14 PIXELS WOULD ENABLE IMAGING A COLLECTION OF GALAXIES**



Technical Approach

To enable science beyond HIFI and GREAT, design, build and advance technical readiness for a 16-pixel 1.9-2.07 THz array receiver

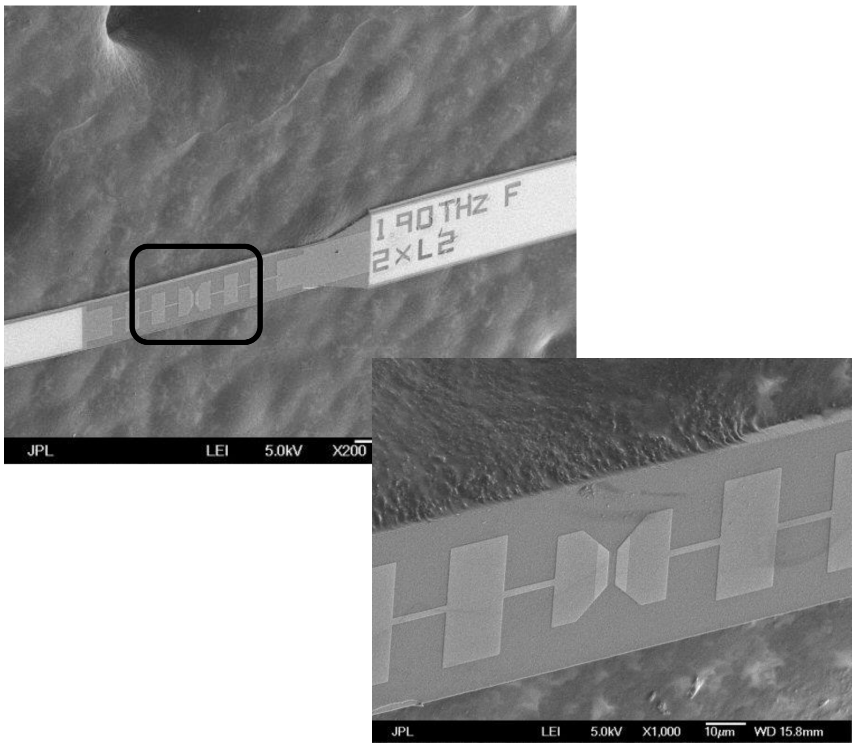
- ✓ **Waveguide based mixers**
- ✓ **Multiple LOs**
- ✓ **QO coupling**
- ✓ **Natural thermal break**
- ✓ **Power per pixel control**
- ✓ **Modular design**



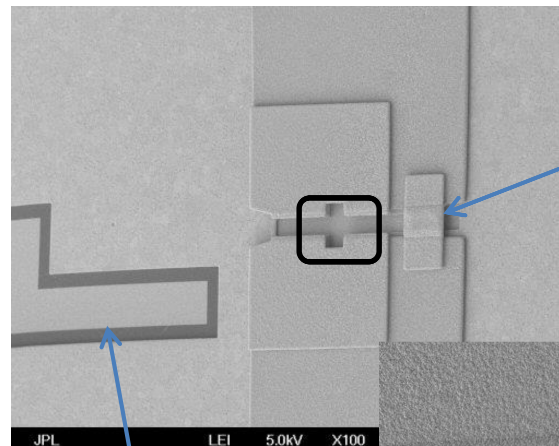
Mixer Design and Development

1.9 THz Mixer Development at JPL

- **HEBs fabricated on thin Silicon On Insulator (SOI) lets us make waveguide chips that work from 500 GHz to 5 THz. Because we etch the chip, we can use a non-rectangular shape.**

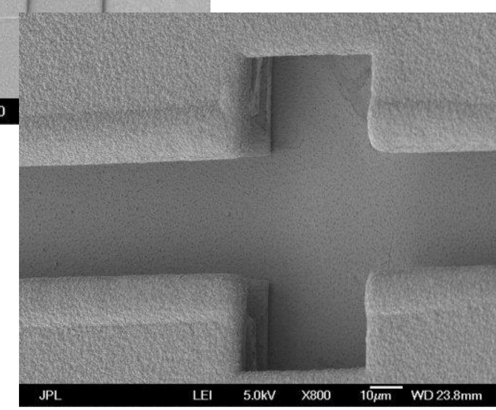


- **Gold plated back pieces are easily mass produced and superior to conventionally machined parts using deep UV lithography. This third generation part has an integrated IF bond pad and suspended ground side bond pad.**

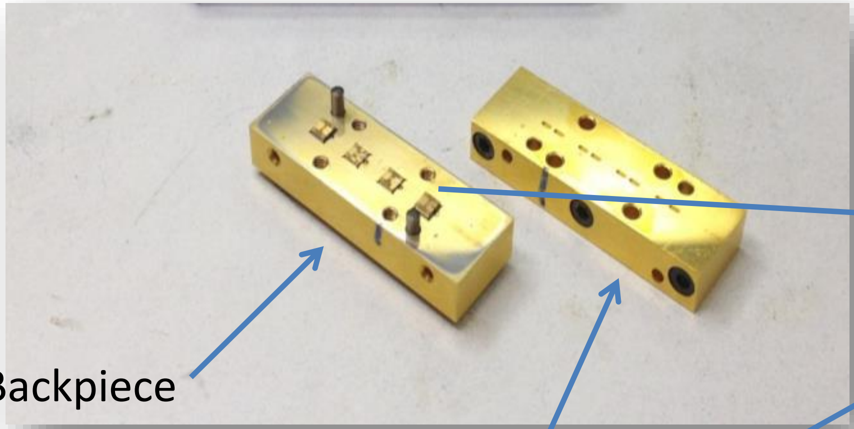


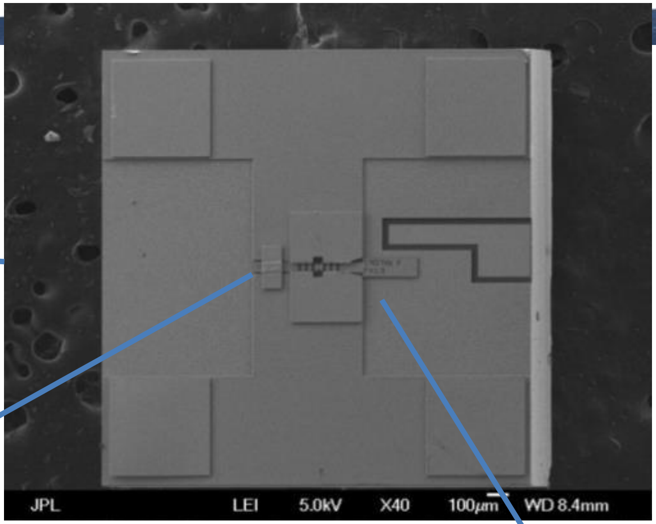
A suspended ground tab will be connected to the mixer using a wire-bond tool.

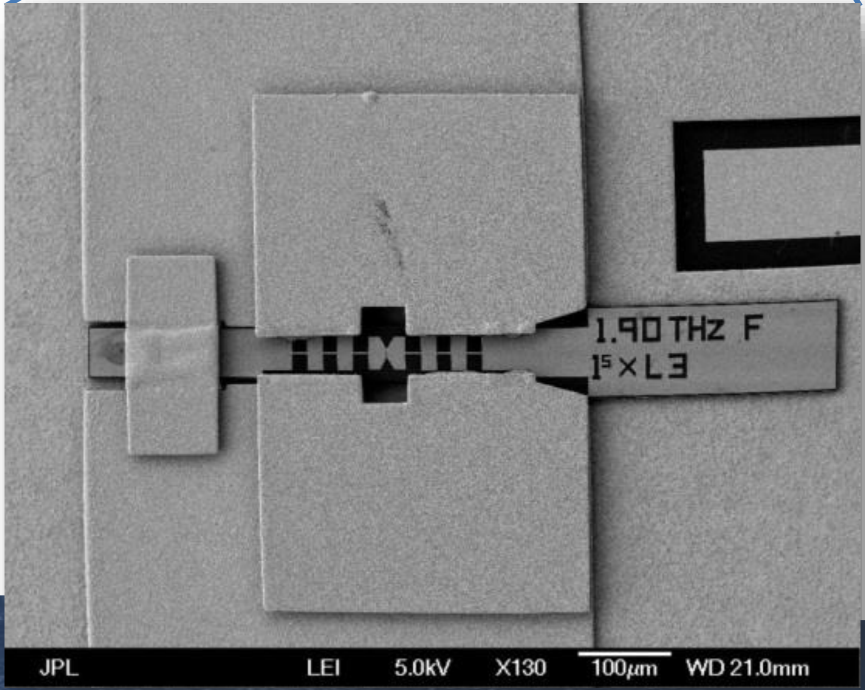
Integrated bond pads will make assembly simpler and more robust.



SOA Waveguide Mixer Block

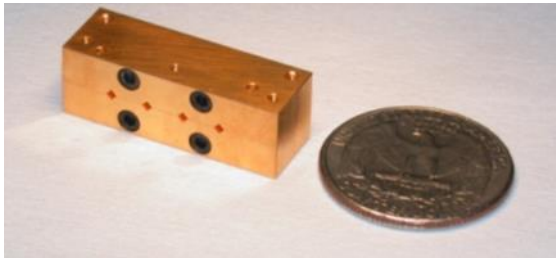




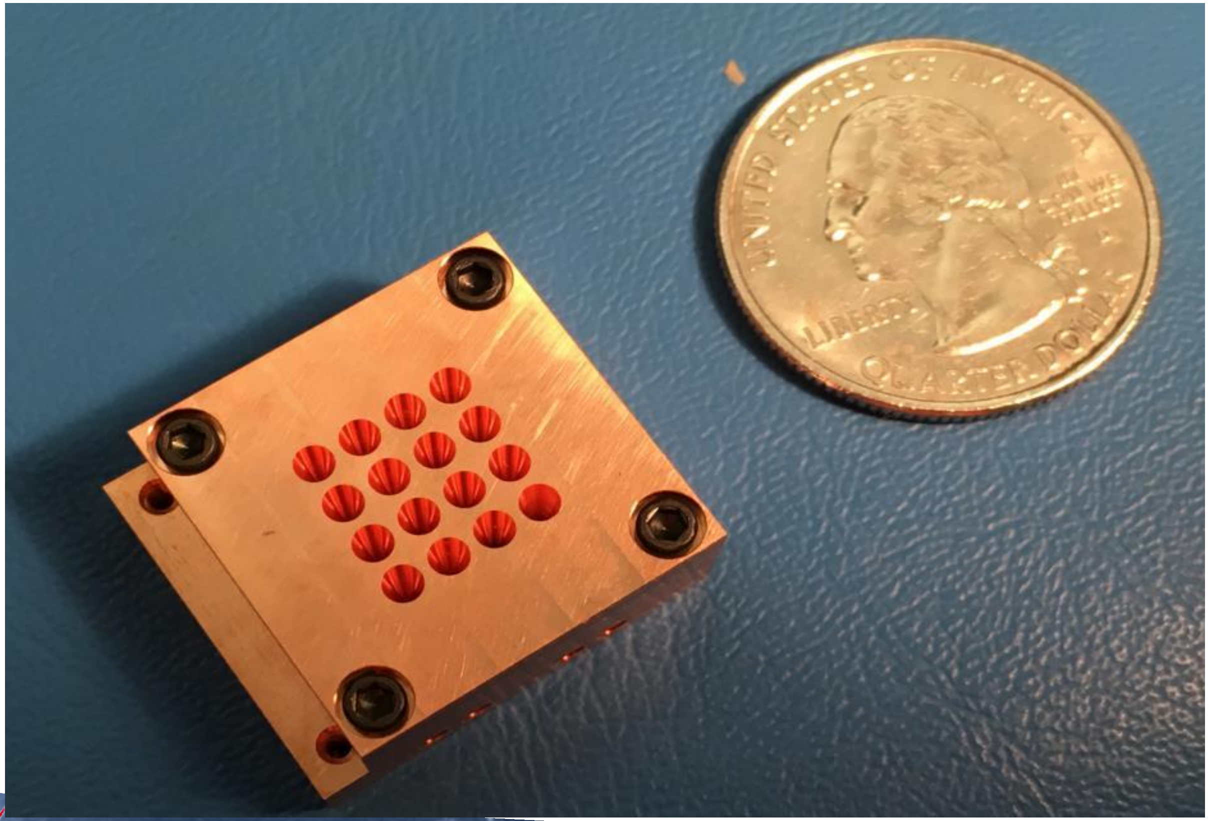


Devices are mounted in a silicon micromachined holder

Multi-pixel mixer blocks

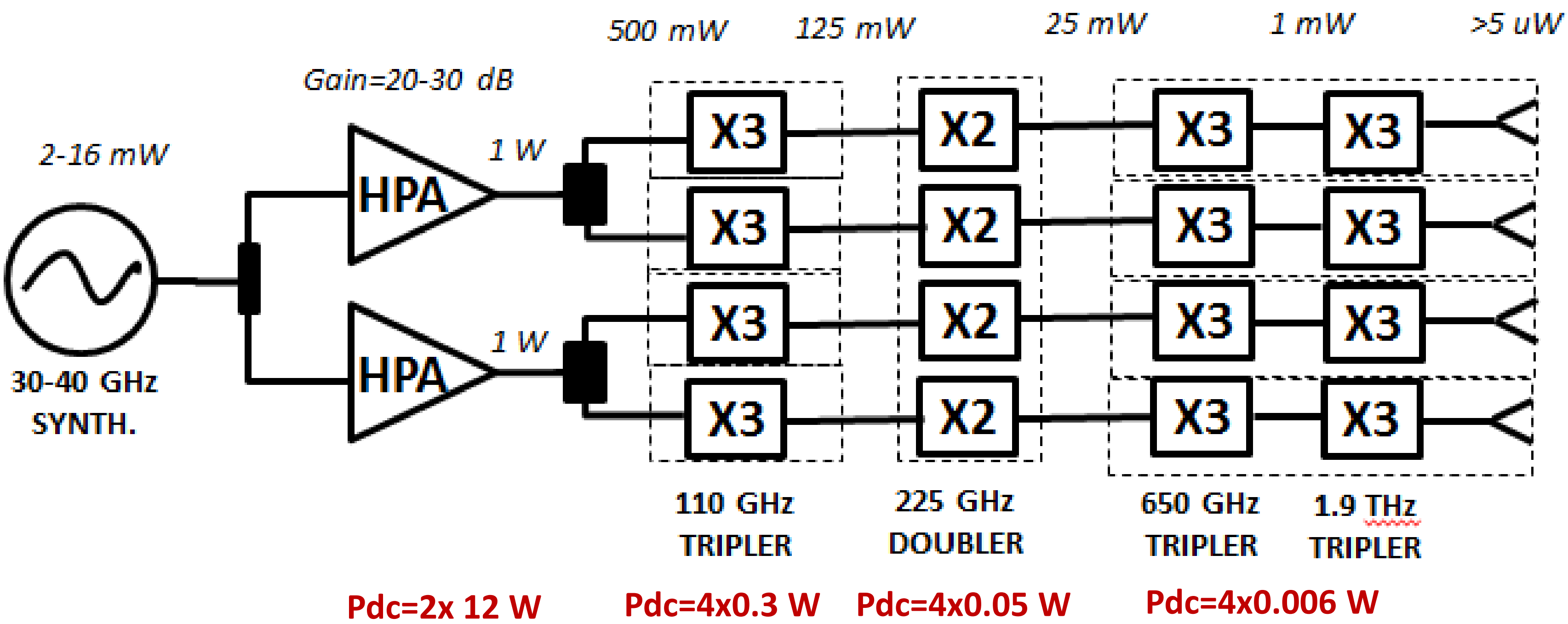


- A 4-pixel mixer block has been designed, fabricated, and tested
- A 16-pixel mixer block has been designed and fabricated



LO Sub-system

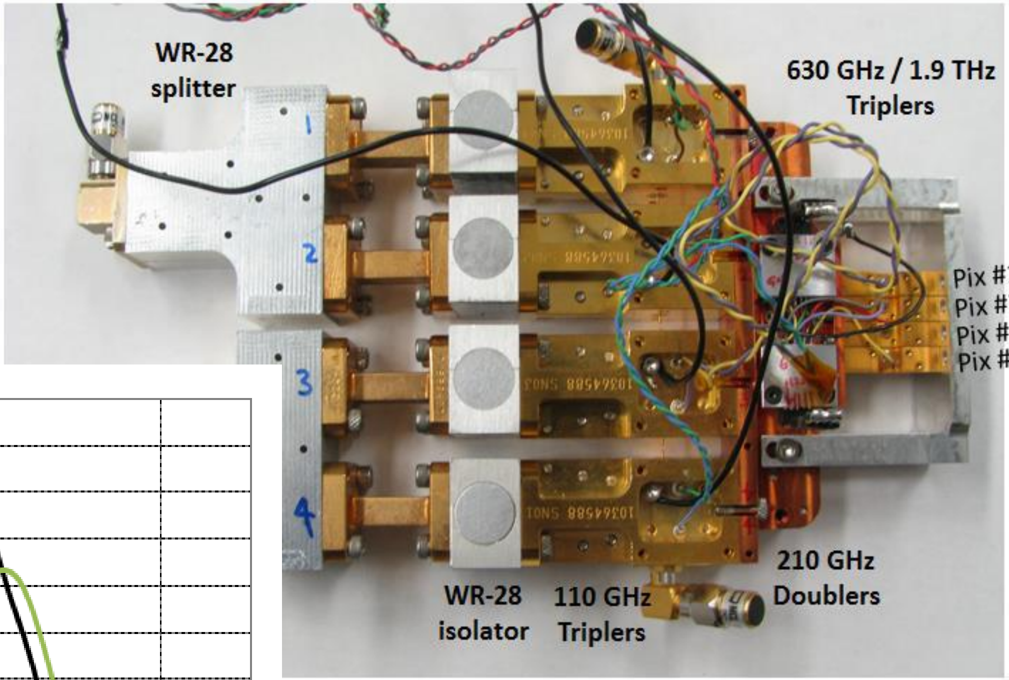
DEVELOPMENT of MULTI-PIXEL LO AT 1.9 THz

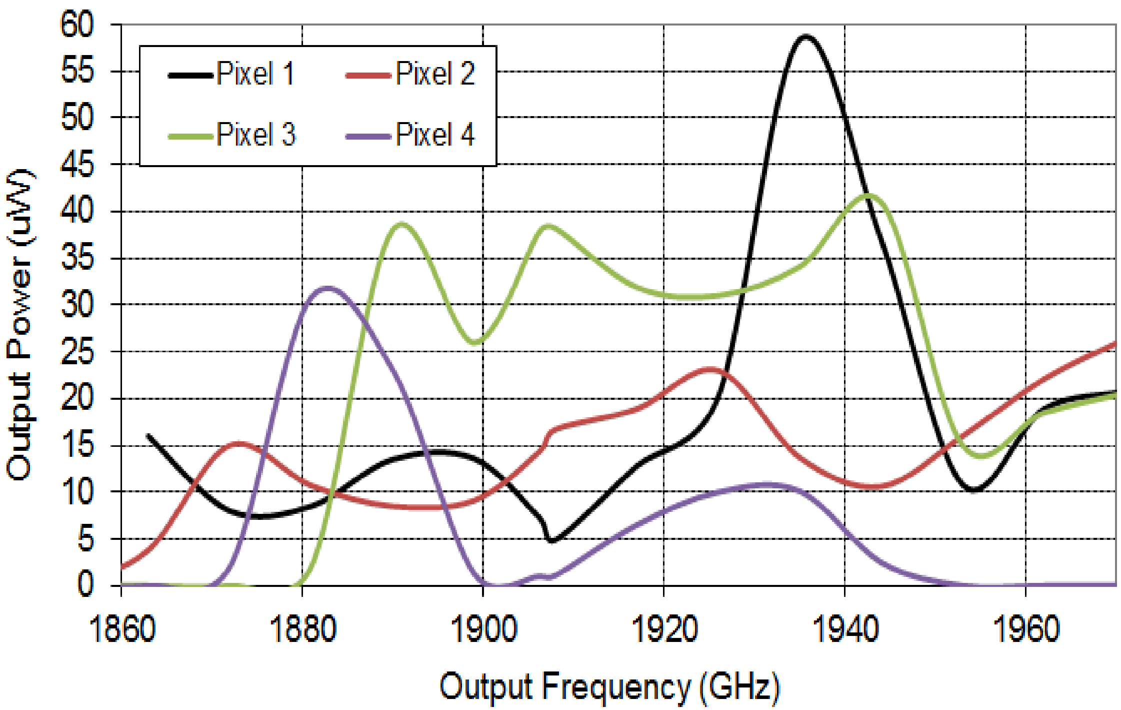


- Different from the scheme used on HIFI
- Based on Ka-band amplifier (easily available but higher DC power)
- Needs development of the first stage tripler
- Second stage doubler is based on four chips
- Third and fourth stage triplers are combined in a single block

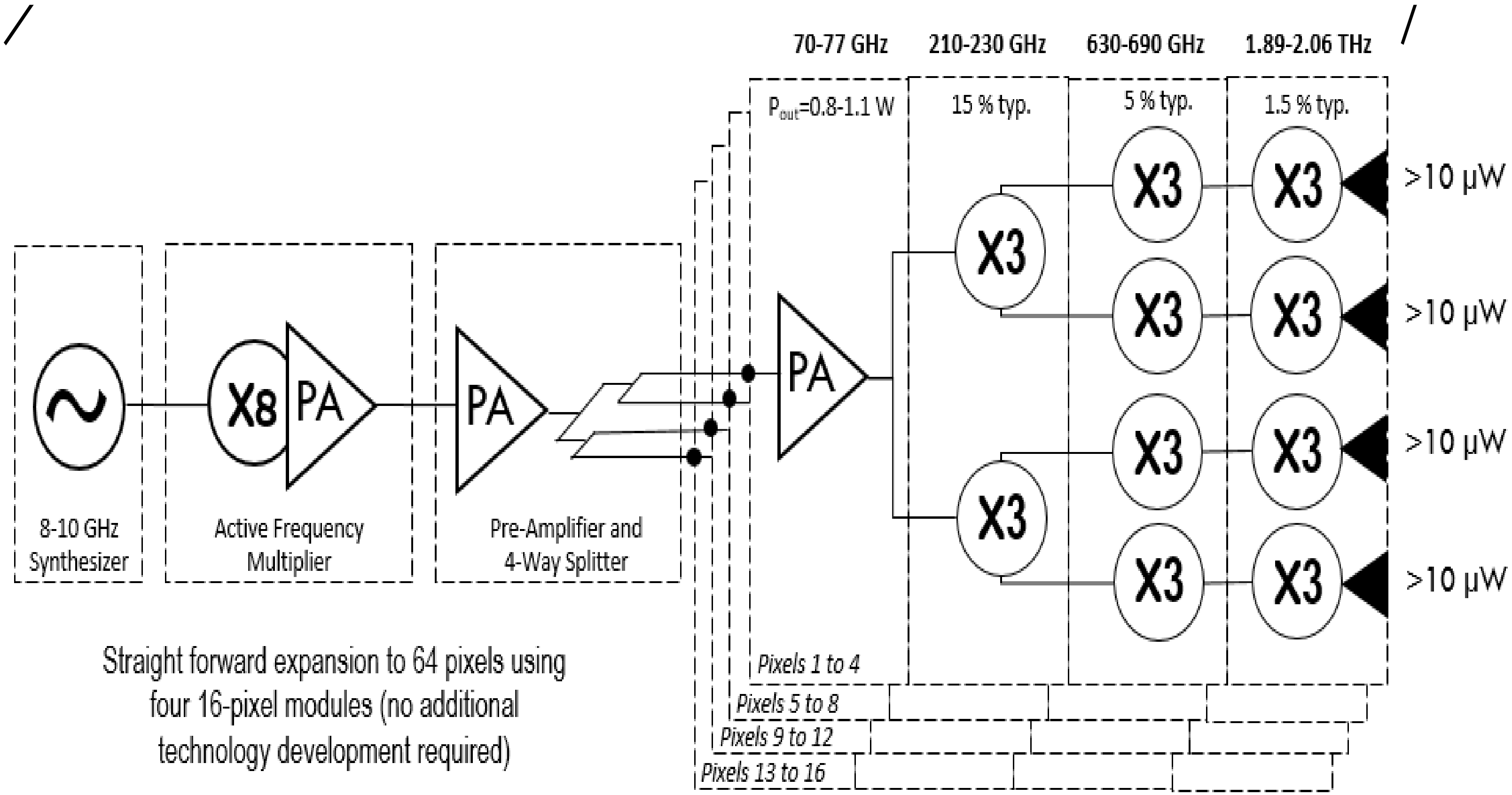
POWER BUDGET
6.35 W/pixel

DEVELOPMENT of MULTI-PIXEL LO AT 1.9 THz: BIASLESS 1.9 THz TRIPLERS





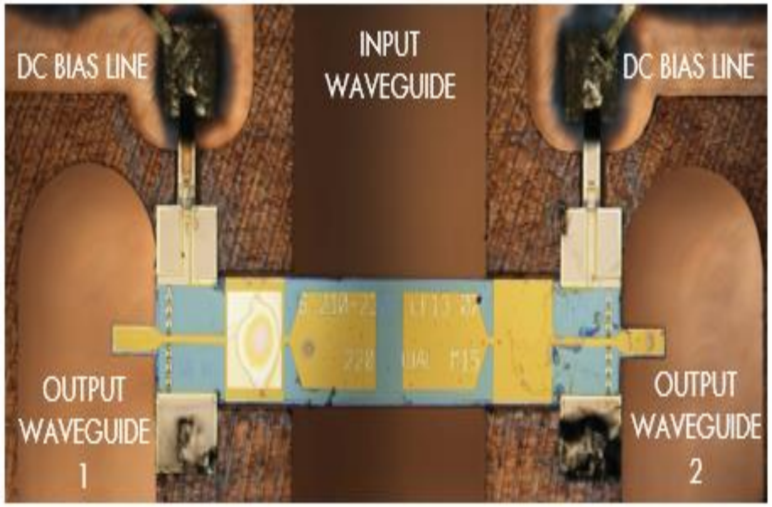
16-Pixel 1.9-2.06 THz LO subsystem

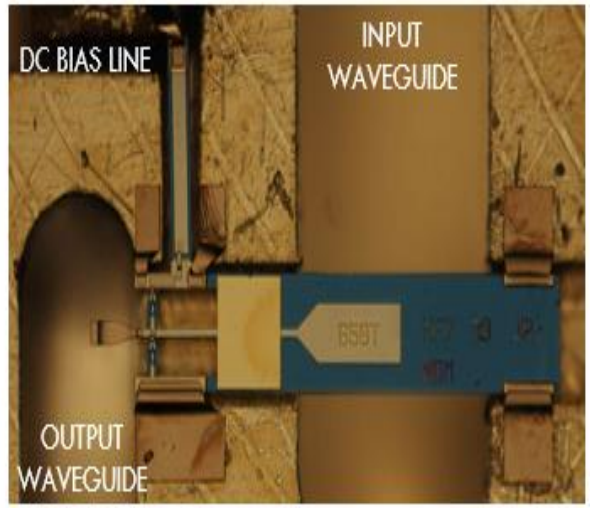


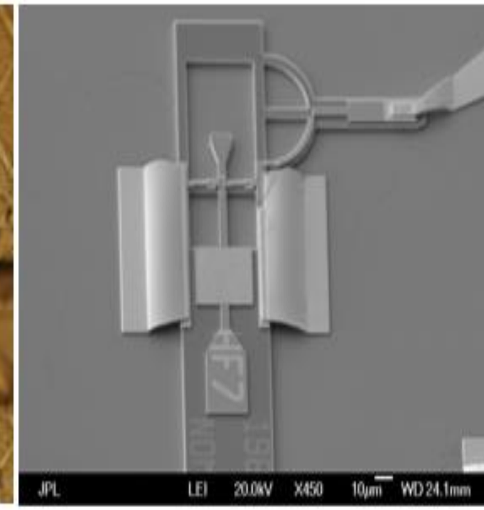
Straight forward expansion to 64 pixels using four 16-pixel modules (no additional technology development required)

Power Consumption= 2.3 Watts/pixel

Optimized Device Designs for Power and Efficiency







1st STAGE: On-chip Power Combined 210-240 GHz Tripler (JPL/Caltech patented technology)

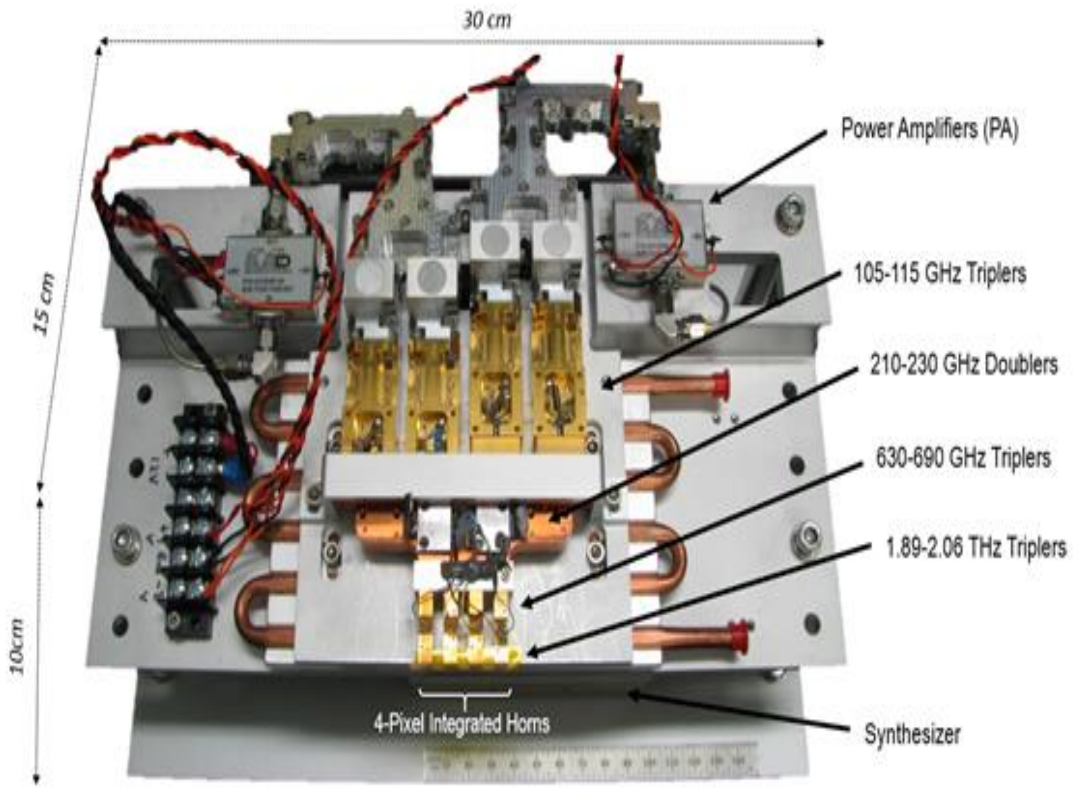
2nd STAGE: High-Power 600-700 GHz Tripler (State-of-the-art)

3rd STAGE: Biasable 1.9-2.06 THz Tripler (First biasable tripler demonstrated beyond 1.5 THz)

All required multipliers (x3x3x3) needed for the 16-pixel LO source have been designed, fabricated and tested under this SAT program.

2nd Generation 4-pixel Chain

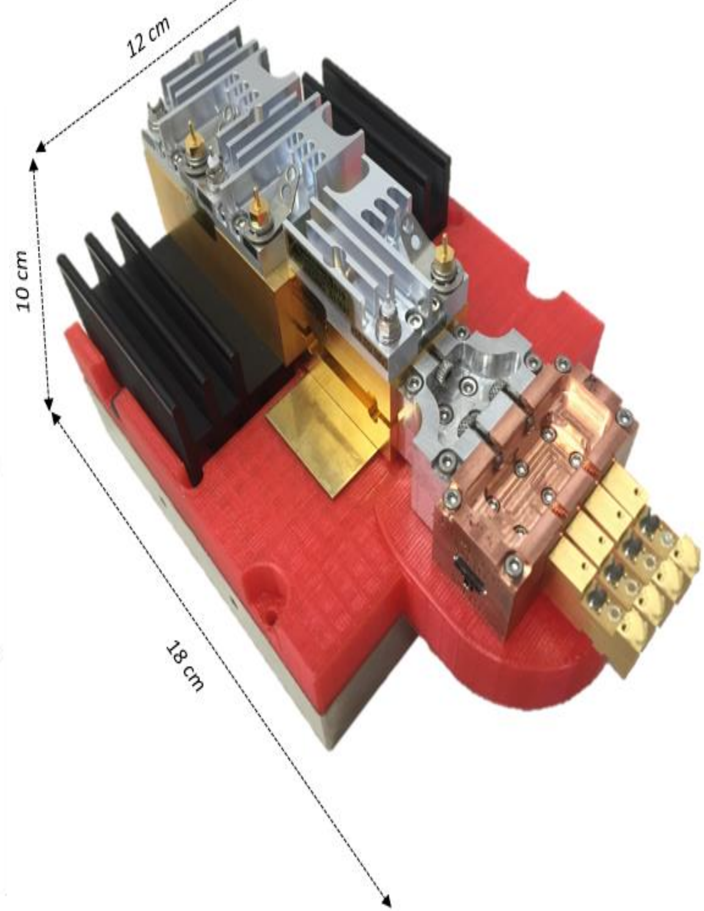
X3X2X3X3 architecture



1.9 THz 4-Pixel Frequency Multiplied Chain delivered by JPL for NASA's Stratospheric Terahertz Observatory, STO-2 (schedule to launch in Dec. 2016).

Power Consumption= 28 Watts/pixel

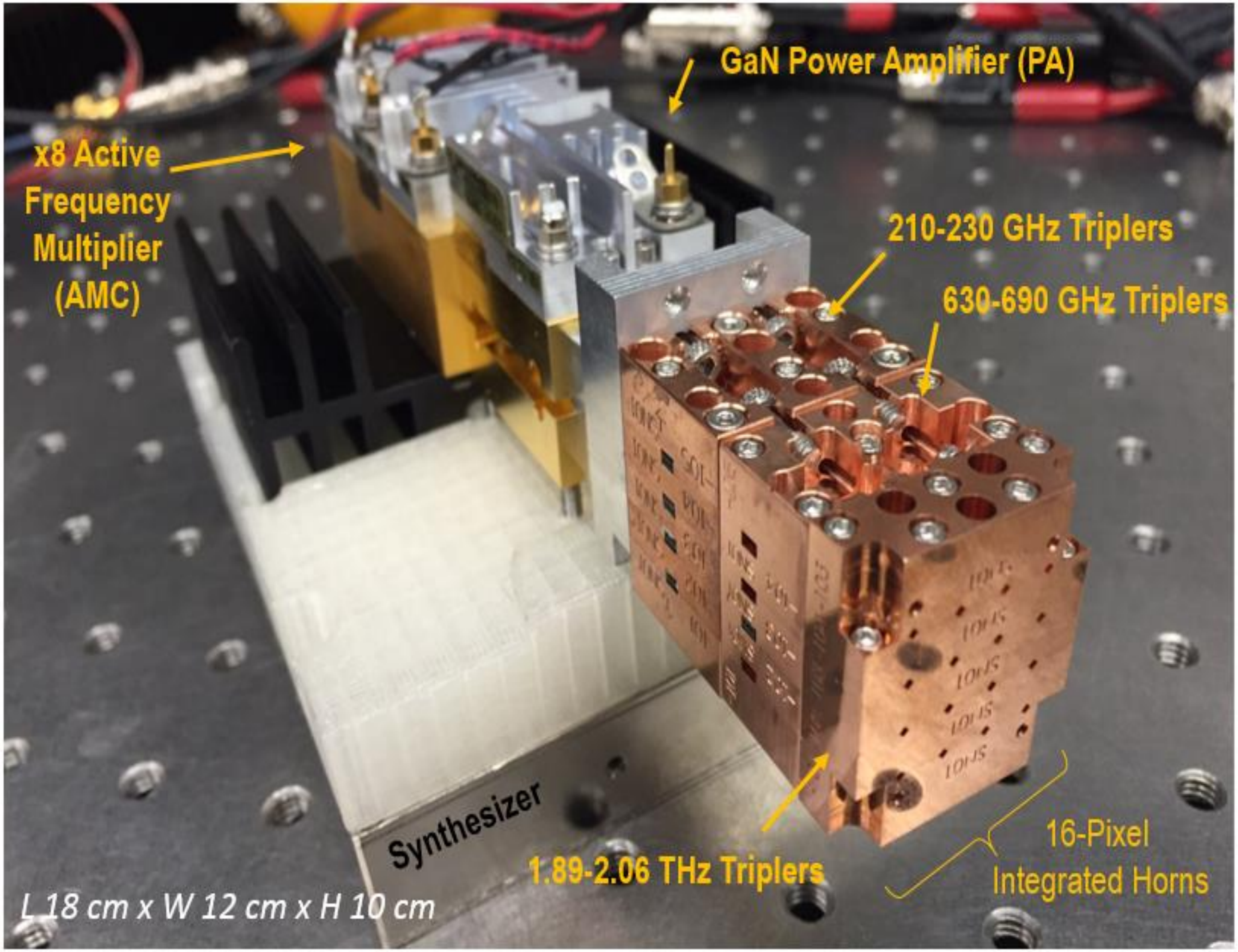
X3X3X3 architecture



2nd Generation 1.9 THz 4-Pixel Frequency Multiplied Chain

Power Consumption= 5.5 Watts/pixel

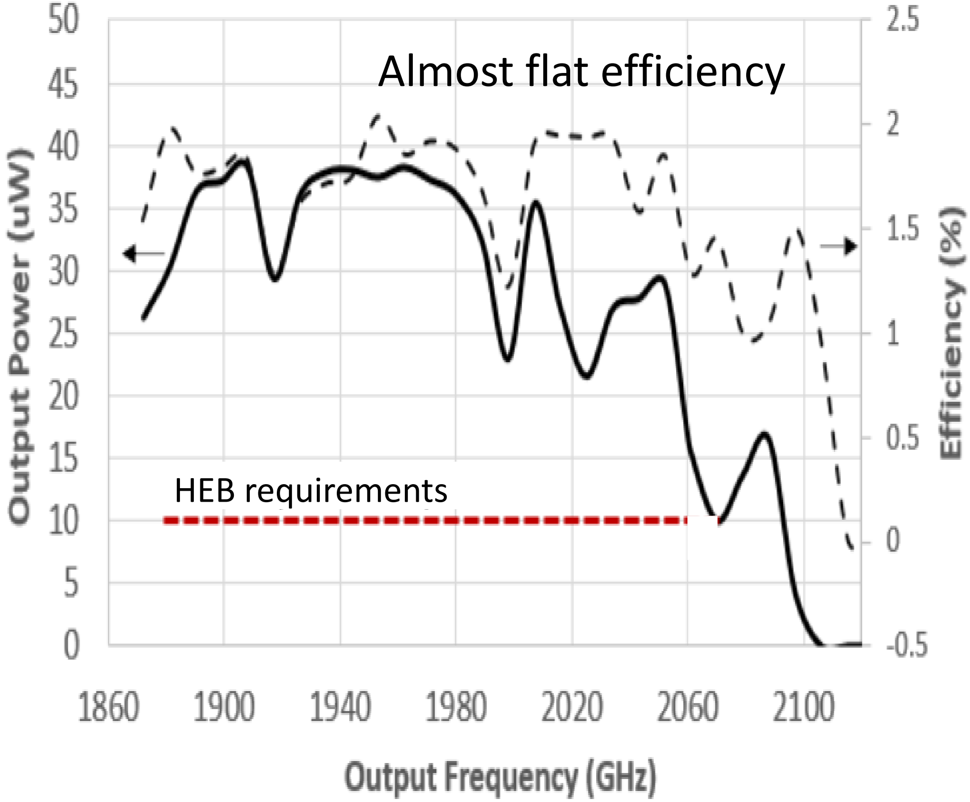
16-Pixel 1.9-2.06 THz LO subsystem



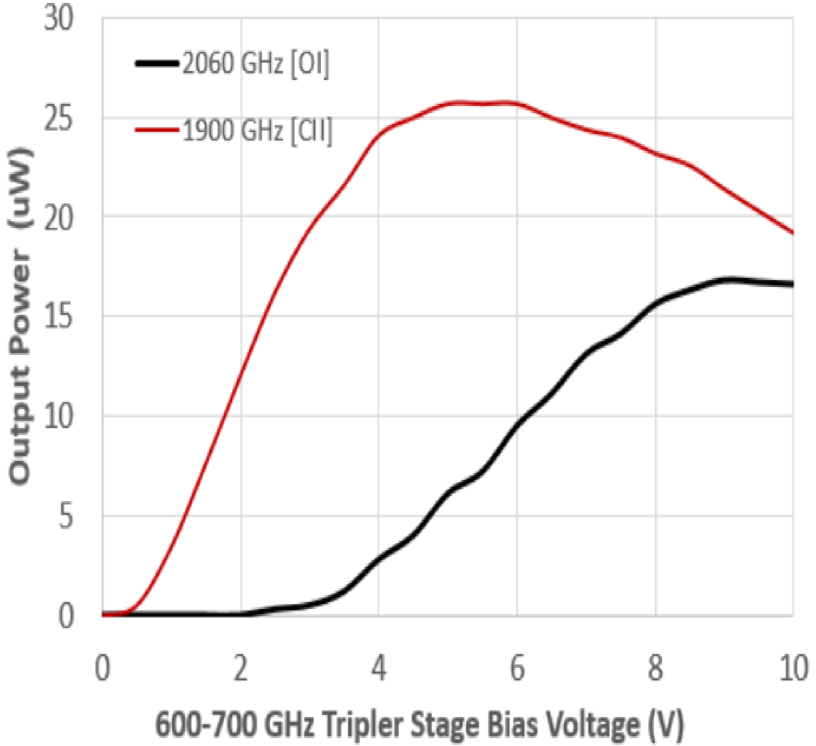
Power Consumption= 2.3 Watts/pixel

LO Chain Typical Performance

High power/large bandwidth source with no cooling required



Individual output power per pixel adjustment



- *Substantial power margin, i.e., reduces critical alignment tolerances*
- *Improves system level stability*
- *Reduces LO noise contribution*
- *Output power control via bias (adjust power per pixel)*

Backend Design and Development

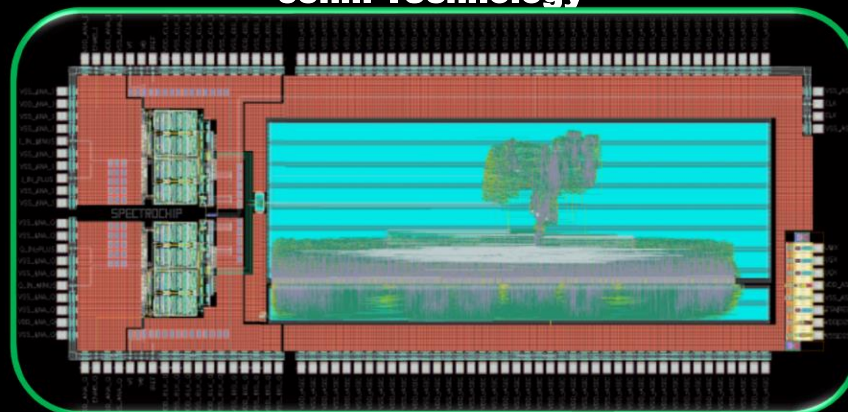
CMOS DSP Compared with FPGA

For array receivers backends pose a technological bottleneck

Existing JPL Spectrometer Processors (FPGA Based)

Performance Metric	Value
Power Usage	30-40 W
Weight	1-2 Kg
Volume	100cm^3
Channel Count	8192-16384
Sample Rate	8-10 GS/s
Unit Cost	$10000

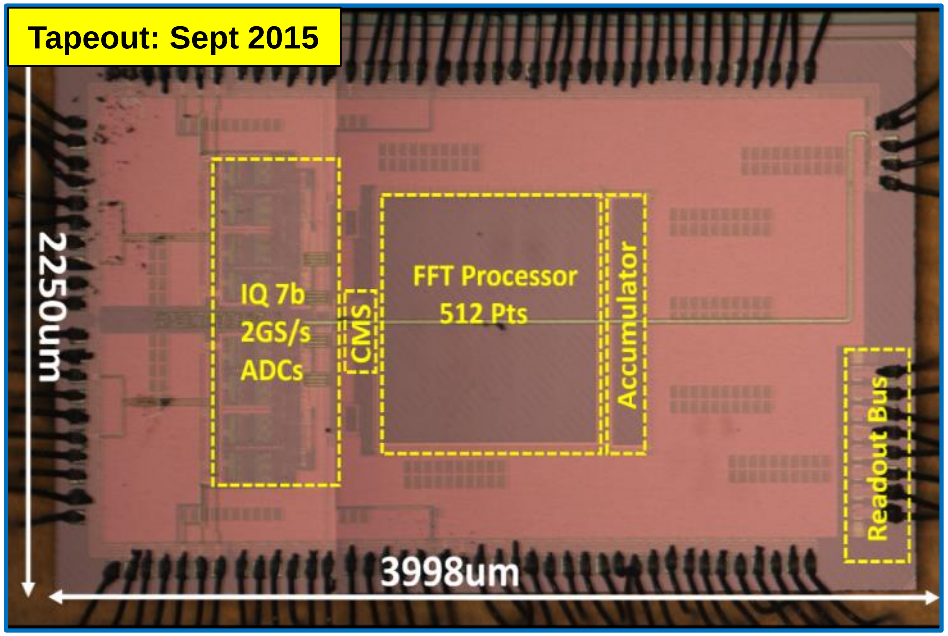
First Generation Proof of Concept CMOS Spectrometer 65nm Technology

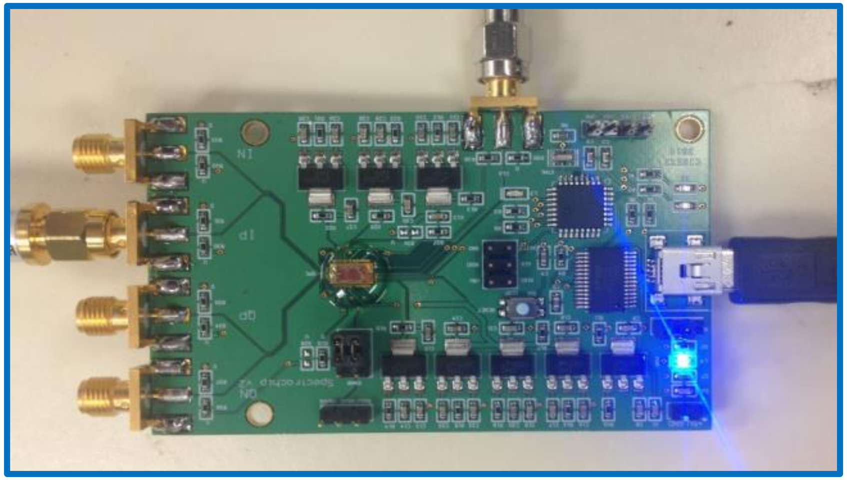


Power Usage	0.3 W
Weight	1-2 g
Volume	1cm^3
Channel Count	512
Sample Rate	2.2 GS/s
Unit Cost	$690 Prototype $0.50 Production

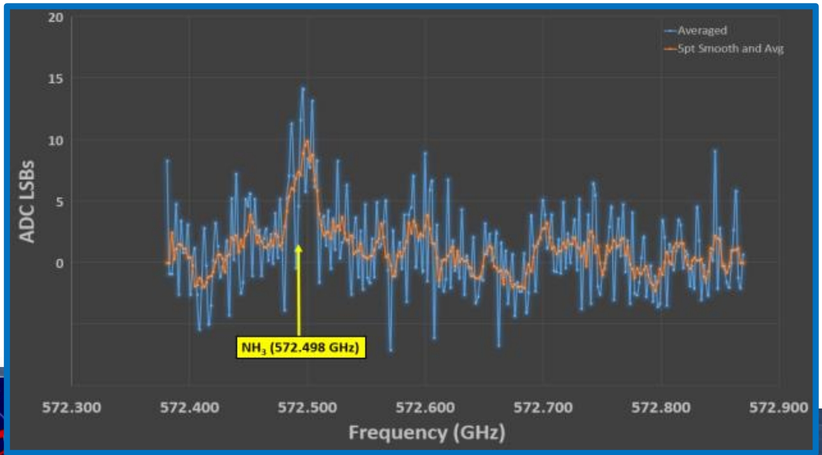
UCLA

Recap of Prior FFT Spectrometer Chip v1 (2014)





Successful NH_3 Gas Cell Test (Jan 2015)



Spectrometer Chip V1 Characteristics

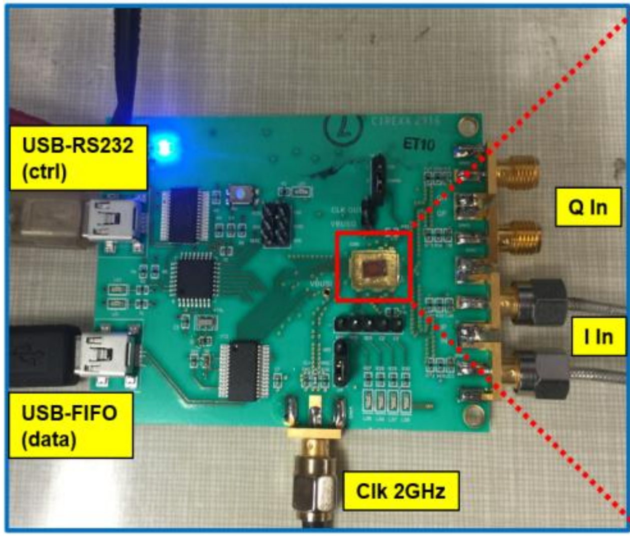
- SSB Spectrometer
- 512 Channels (256 if your mixer output is not IQ)
- Hanning Window
- 750 MHz of input bandwidth
- 188mW Power Consumption

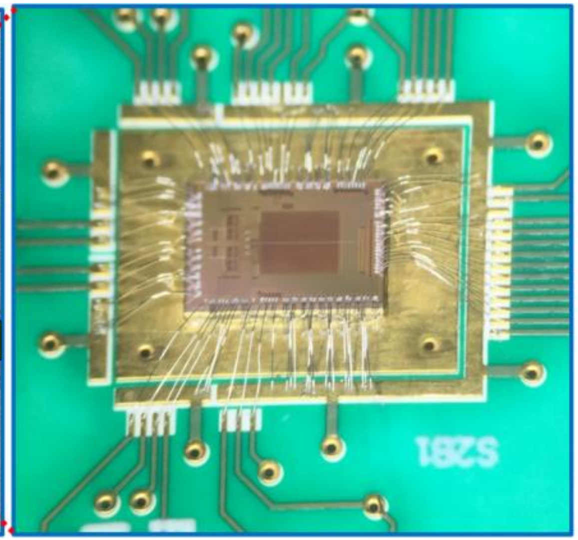
Performance Issues found:

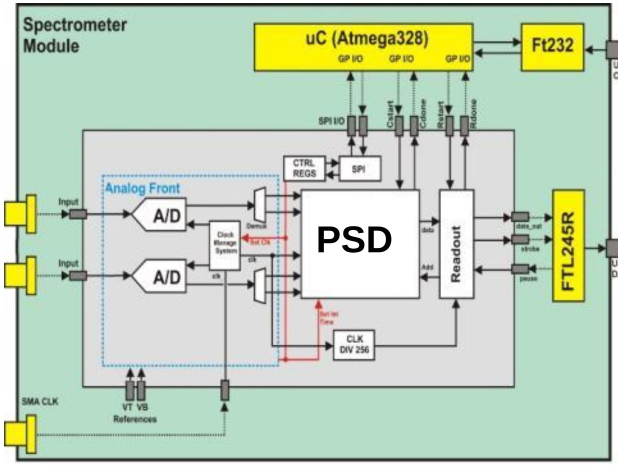
This was our very first prototype in this work so evaluation led to identifying required improvements in future versions:.

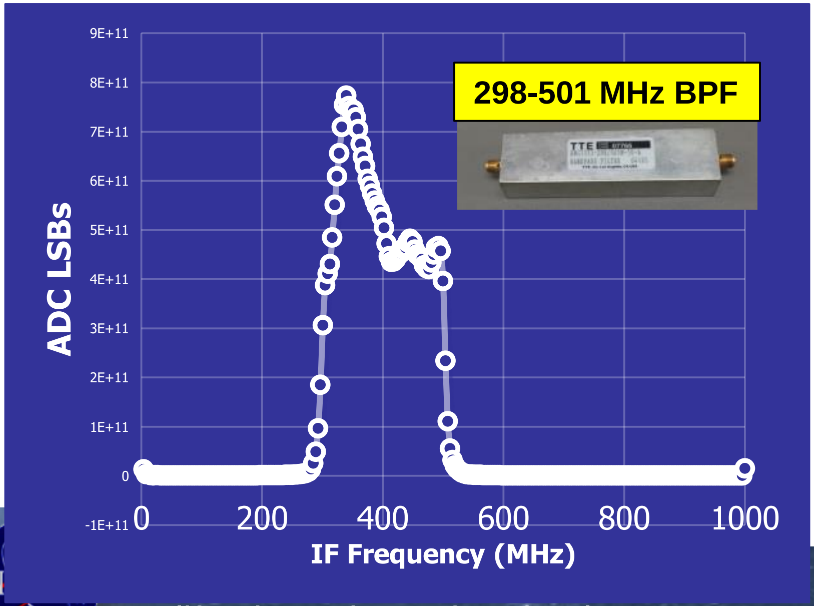
Chip functions exactly as designed but it has a serial bus interface so the readout is very slow inside the larger system. Low measurement duty cycle (about 5%)

New FFT Spectrometer Chip v2







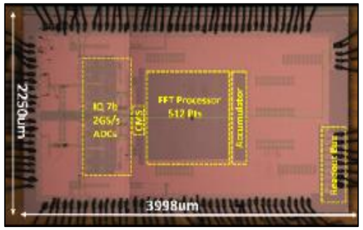


Spectrometer V2 Chip Characteristics

- Very similar to the previous chip but changes the readout from a serial connection (56Kb/s) to a full USB2.0 on-chip controller (512 Mb/s) to improve the duty cycle
- Duty cycle is now measured to be 99.5% for a 1 second integration time.
- Also improves on the ADC to push the bandwidth up to 1000 MHz

UCLA/JPL CMOS Spectrometer Chip Roadmap

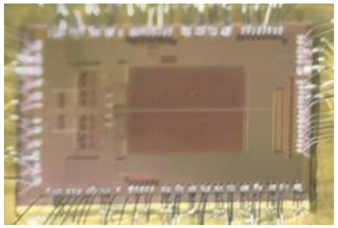
Existing Spectrometer Demonstrations with UCLA



Spectrometer V1

Developed 2015

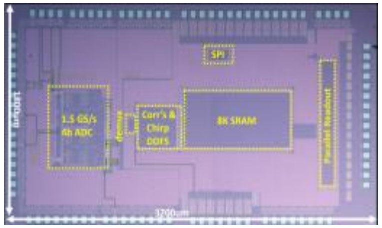
- FFT Based
- 750 MHz Bandwidth
- 512 Channels
- UART Readout
- 188mW



Spectrometer V2

Developed 2016

- FFT Based
- 1 GHz Bandwidth
- 512 Channels
- High Speed Readout
- 220mW

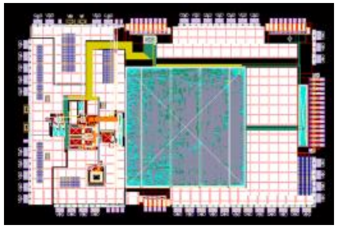


Spectrometer V3

Developed 2016

- DCTS Based
- 500 MHz Bandwidth
- 1024 Channels
- High Speed Readout
- 168mW

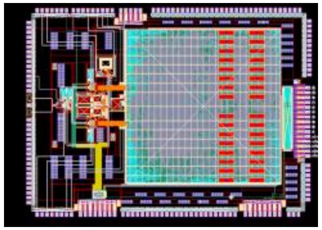
Proposed in Adrian Tang's FY'17 APRA (ranked in "selectable" category)



Spectrometer V4

(if APRA is funded)

- FFT Based
- 1500 MHz Bandwidth
- 2048 Channels
- High Speed Readout
- 250mW



Spectrometer V5

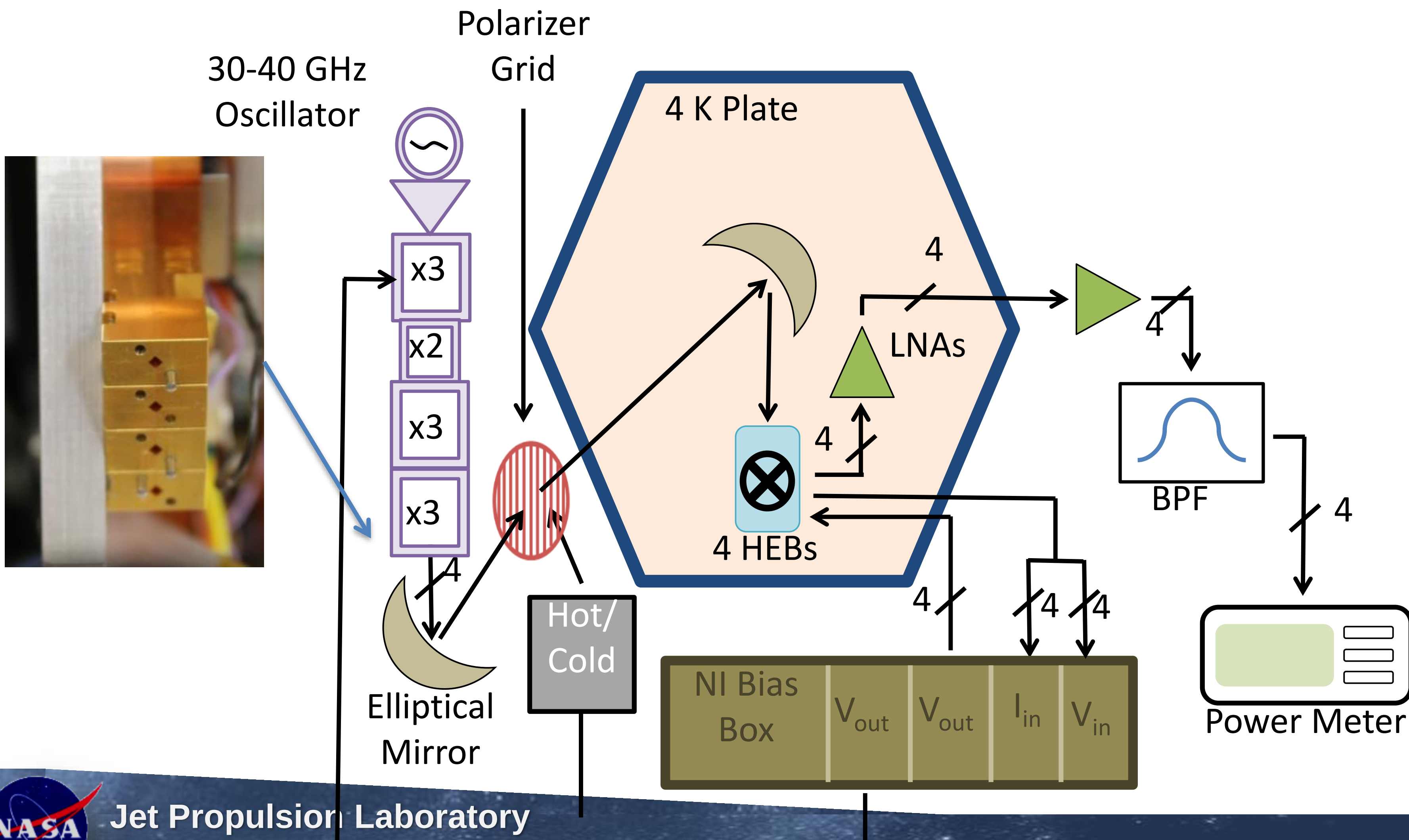
(if APRA is funded)

- FFT Based
- 3000 MHz Bandwidth
- 4096 Channels
- High Speed Readout
- 330mW

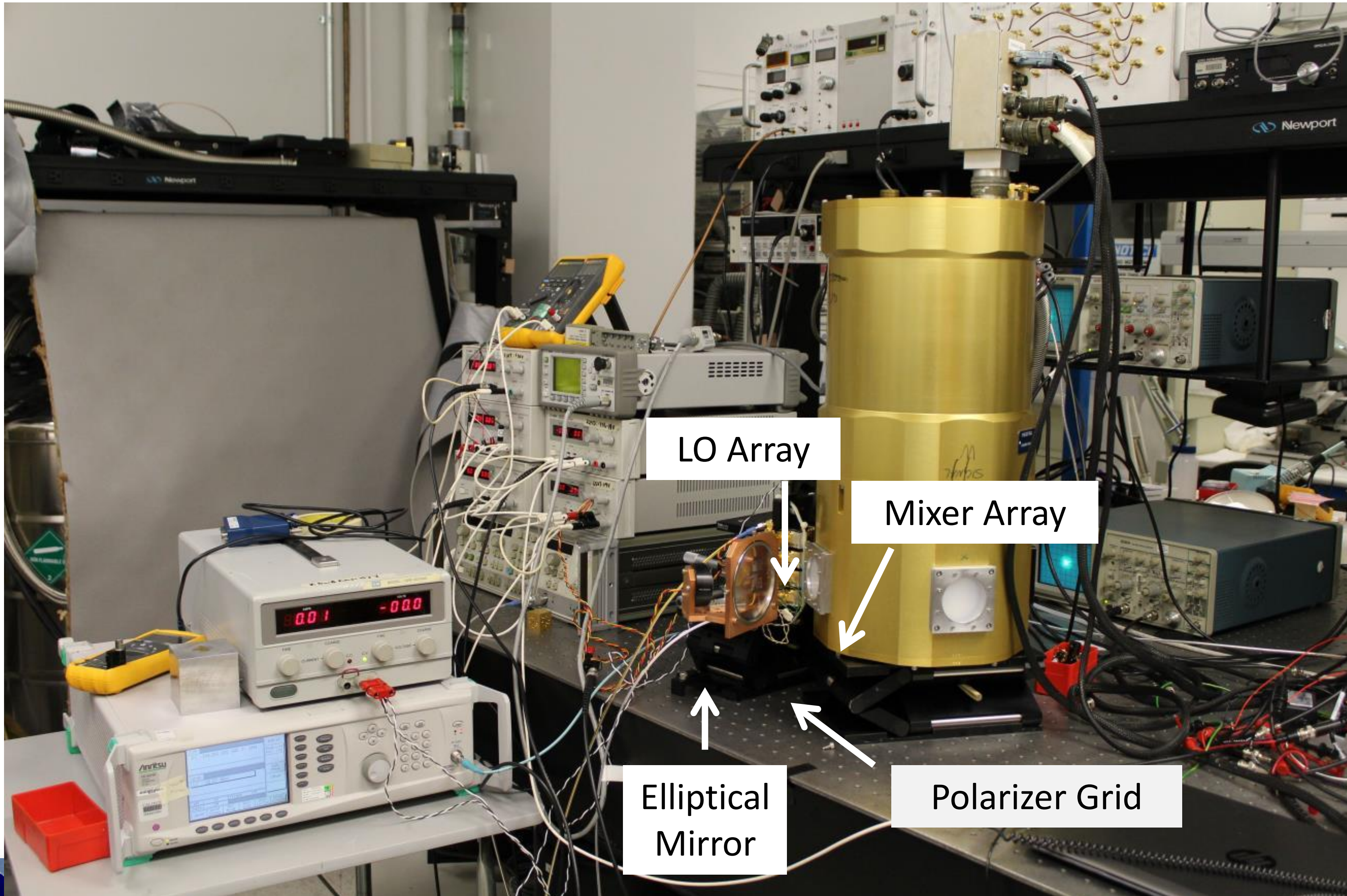
- Making steady progress in all aspects of back end processing: bandwidth, channel count and readout speed.
- Requires significant system-on-chip (SoC) capabilities: Large scale calibration, SoC Planning, intense CAD design and verification tools, large libraries of proven circuit blocks and previously existing IP: SRAMs, ADCs, Clock Controllers, USB controller cores, …

Receiver System
Assembly and Testing

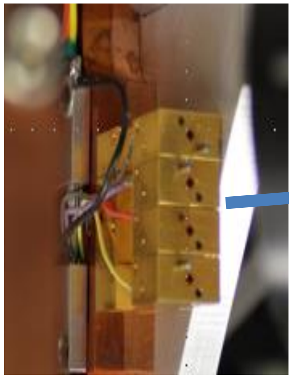
Receiver Setup



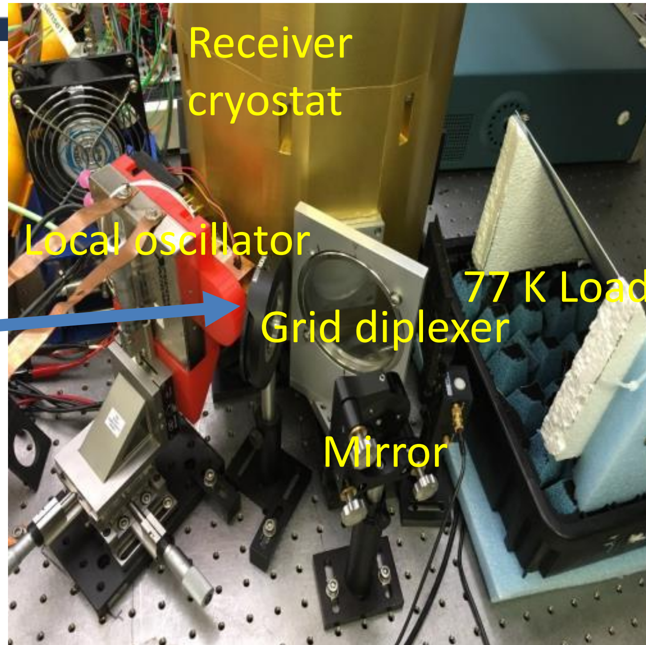
Lab Setup

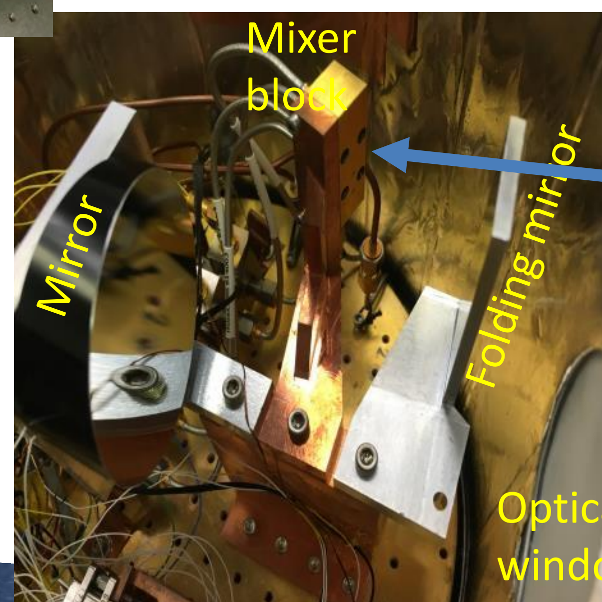


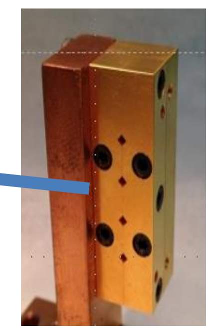
LO-mixer coupling accomplished by 2-mirror GBT



4-pixel
LO

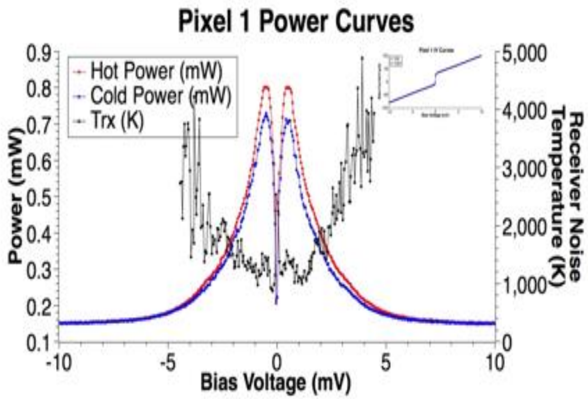


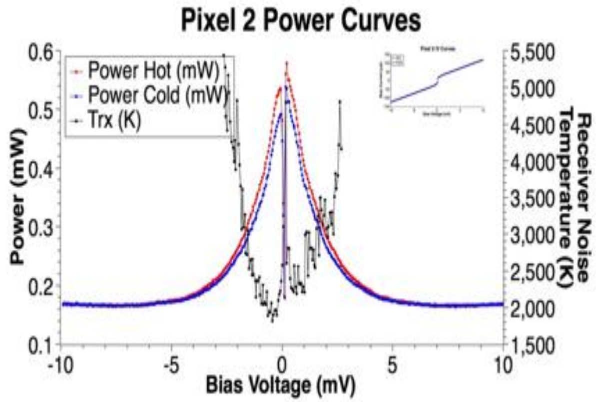




4-pixel
mixer

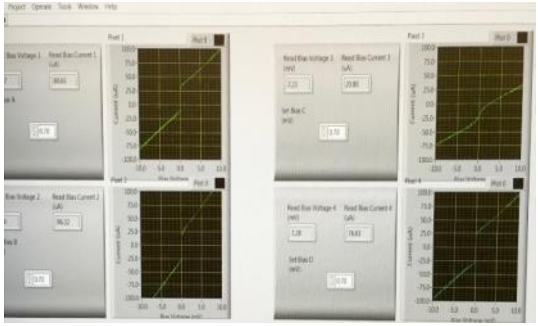
Multi-pixel Receiver measurements

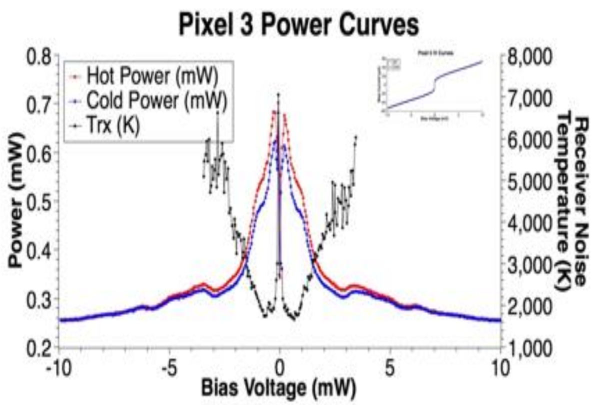


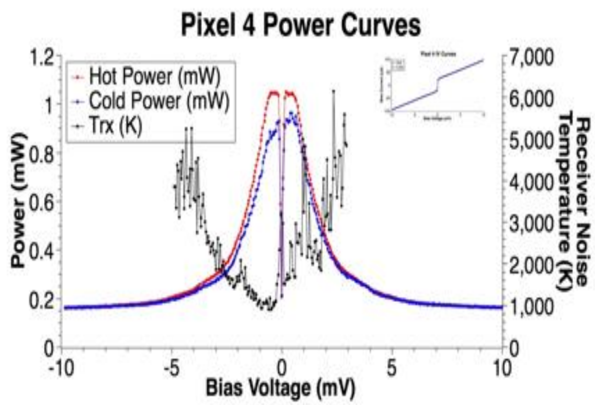


Best Y-Factor: 1.21, T_{rx} = 900 K

Best Y-Factor: 1.11, T_{rx} = 1800 K

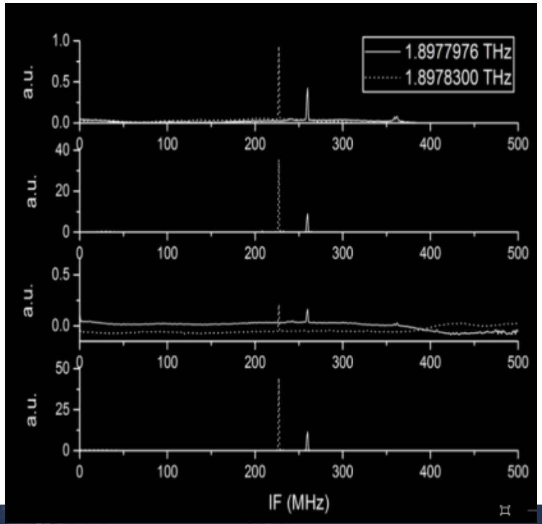




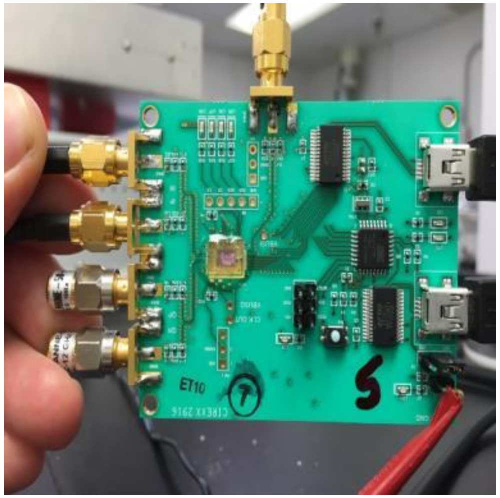


Best Y-Factor: 1.12, T_{rx} = 1700 K

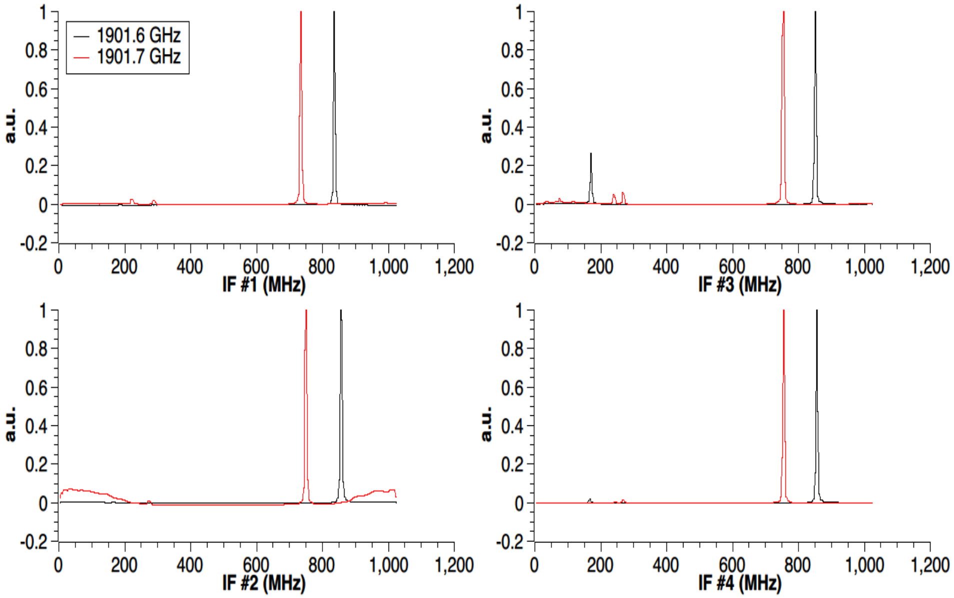
Best Y-Factor: 1.21, T_{rx} = 900 K

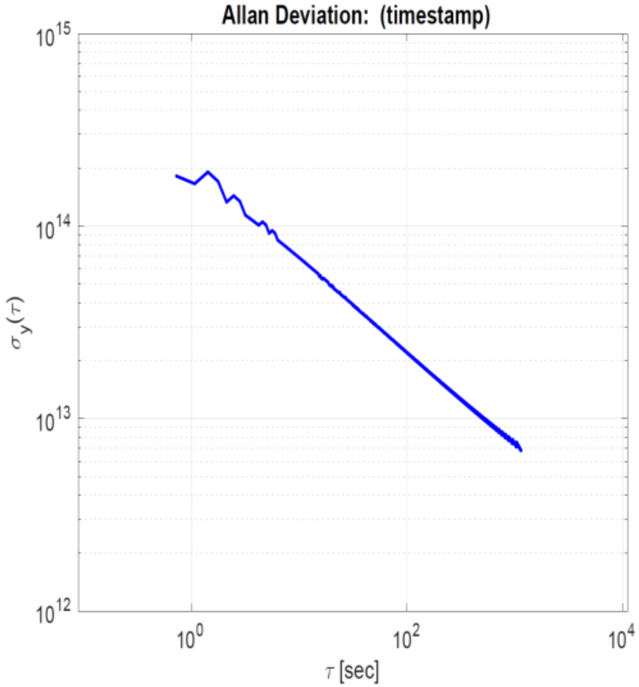


End-to-End Demonstration



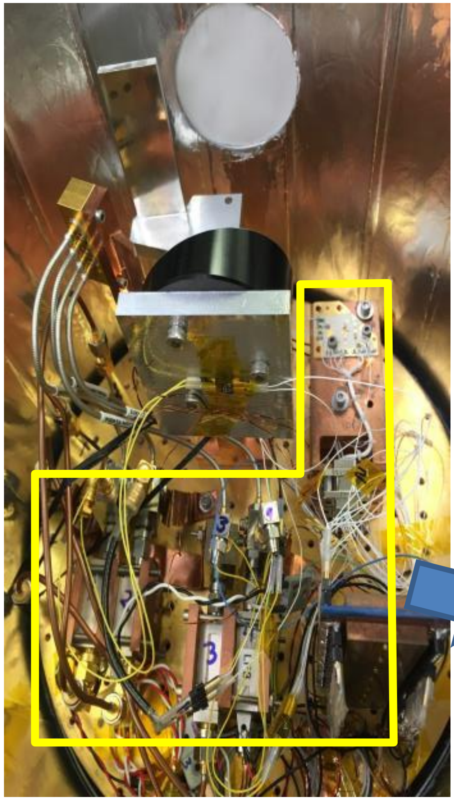
Prototype 1-GHz 256-channel spectrometer



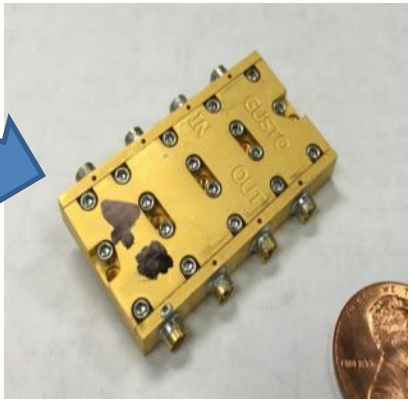


Preliminary stability measurements indicate that the noise integrates down as expected

Towards a compact expandable 16-pixel receiver system

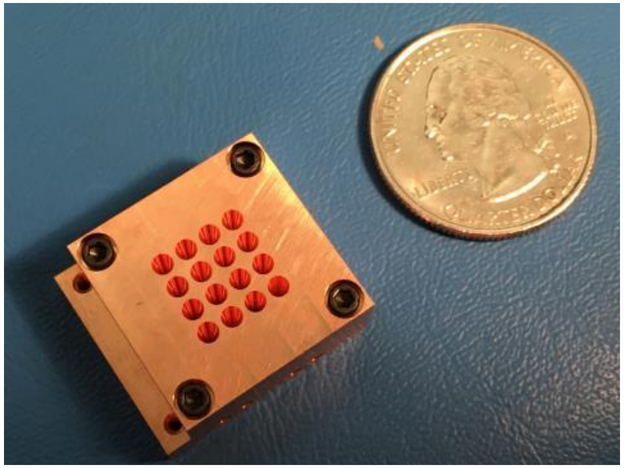


Discrete LNAs, bias tees and circuit cards used.



0.5-6 GHz 4-channel SiGe LNA with integrated bias-tee

16-pixel mixer block with drilled horns (Produced by C. Groppi ASU)



The GREAT 14-pixel mixer array is built from discrete components

Summary

- **Current status of THz array receivers:**
  - 16-pixel LO subsystem has been assembled
    - Record output power
    - Output power is controlled
    - Compact low power approach
    - Modular, room temperature operation
  - 2nd generation backend spectrometer in advanced CMOS technology demo’ed
    - <250 mW of DC power
    - <15 g (on PCB including controllers)
  - 4-pixel receiver system demo’ed
    - SOA performance with modular design